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HL9469-PCIe8.0 Broadband Z-matched Pick-off Tee

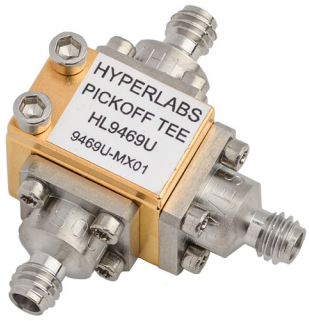
(Designed for PCIe® 8.0 compliance testing)

Key Features and Technical Specifications[1]

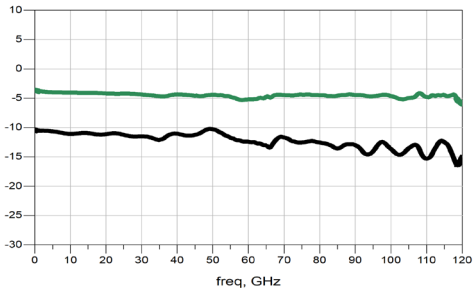
Bandwidth	DC to 110 GHz, thru and pick-off lines
Insertion Loss See *Fig. 1*	4.5 ± 1 dB, thru line 11.0 dB, pick-off line
Return Loss *See Fig. 2*	< 15 dB, f < 100 GHz < 10 dB, 100 GHz ≤ f < 110 GHz
Amplitude Match (opt. -M only)	± 0.5 dB, DC < f ≤ 60 GHz ± 0.75 dB, 60 GHz < f ≤ 110 GHz Thru line only
Phase Match (opt. -M only)	± 5°, DC < f ≤ 60 GHz ± 10°, 60 GHz < f ≤ 110 GHz Thru line only
Rise Time	3 ps, thru 4 ps, pick-off
Group Delay *See Fig. 3*	≈ 105 ps, thru line (opt. -JJJ) ≈ 110 ps, thru line (opt. -JPJ) ≈ 110 ps, pick-off line (all opts.)
Input Power	20 dBm (24 dBm max)[2]
Impedance	50 Ω, all ports
Connectors	1.0 mm jack, all ports (opt. -JJJ) 1.0 mm jack, Thru 1 and Pick-off; 1.0 mm plug, Thru 2 (opt. -JPJ)
Unit Dimensions	28.4 x 23.1 x 13.59 mm 1.140” x 0.908” x 0.535”
Weight	12.5 g (0.44 oz.)
Operating Temp.	-40° to +50° C
RoHS Compliant	Yes
REACH Compliant	Yes
Warranty	1 year, repair or replacement

1 - The specifications in this table are typical using the standard connector configuration (-JPJ, jack/plug/jack).

2 - Long-term power handling testing is ongoing. The preliminary specification is 20 dBm.



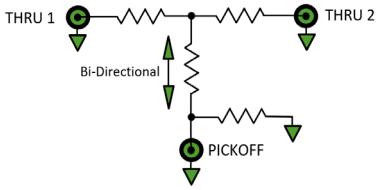
HL9469-PCIe8.0, option -U-JPJ



Typical Insertion Loss on thru and pick-off lines of HL9469-PCIe8.0 (opt. -JPJ); see also Fig. 1

DEVICE PORT ASSIGNMENTS

For the purposes of this datasheet, the below port assignments are used.



PRODUCT SUMMARY

The HL9469-PCIe8.0 is an impedance-matched pick-off tee with a flat frequency response from DC to 110 GHz on the thru line and 110 GHz bandwidth on the pick-off line.

It is suitable as a trigger source with minimum perturbation of the thru signal path. It can be used in 224 Gbps PAM4 communication systems.

Since the pick-off tee is bi-directional, a typical application is to inject noise on the pickoff port into the original signal. This is useful for compliance testing.

This pick-off tee is designed with reduced pulse dispersion to allow for sinusoidal interference (SI) injection without degrading PAM4 signals such as that required for future PCIe® 8.0 compliance testing using 256 GT/s lanes.

Digital oscilloscope applications include pre-scaler triggering, synchronization, and clock/data recovery.

Some specificatons are only applicable to matched pairs of devices and are labeled accordingly.

MODELS & OPTIONS

The following model is available:

HL9469-PCIE8.0, 110 GHz

The following options and configurations are available for this product:

-M, matched pair

-U, unmatched part(s)

-JJJ, jack (female), all ports

-JPJ, jack (female) thru in and pick-off; plug (male) thru out

HL9469-PCIe8.0 Insertion Loss

Figure 1 shows the typical insertion loss of the HL9469-PCIe8.0 along the thru and pick-off lines from DC to 120 GHz.

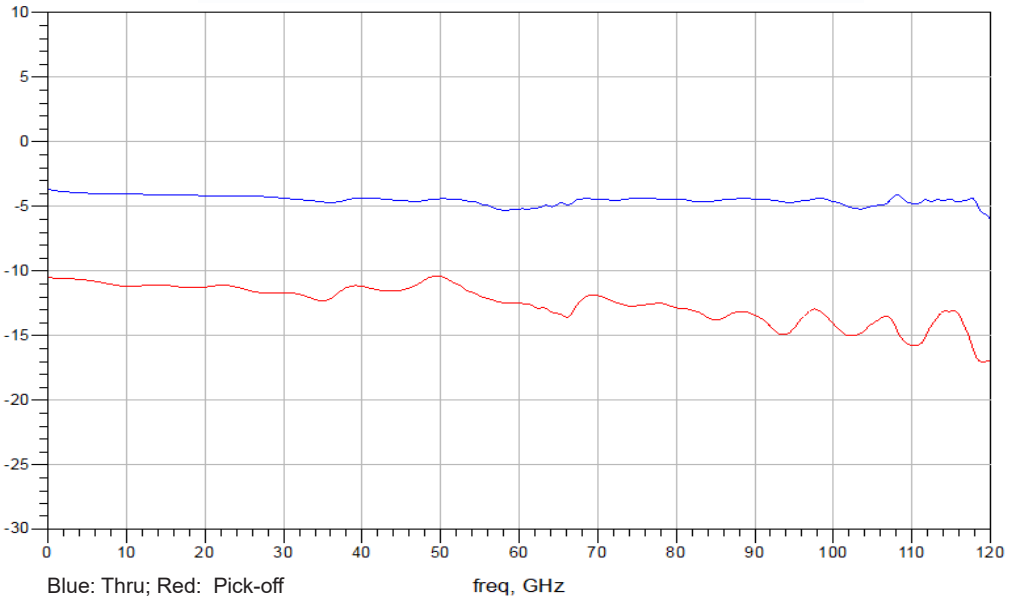


Figure 1: HL9469-PCIe8.0 Insertion Loss (opt. -JPJ)

HL9469 Return Loss

Figure 2 shows the typical return loss of all ports of the HL9469-PCIe8.0 from DC to 120 GHz.

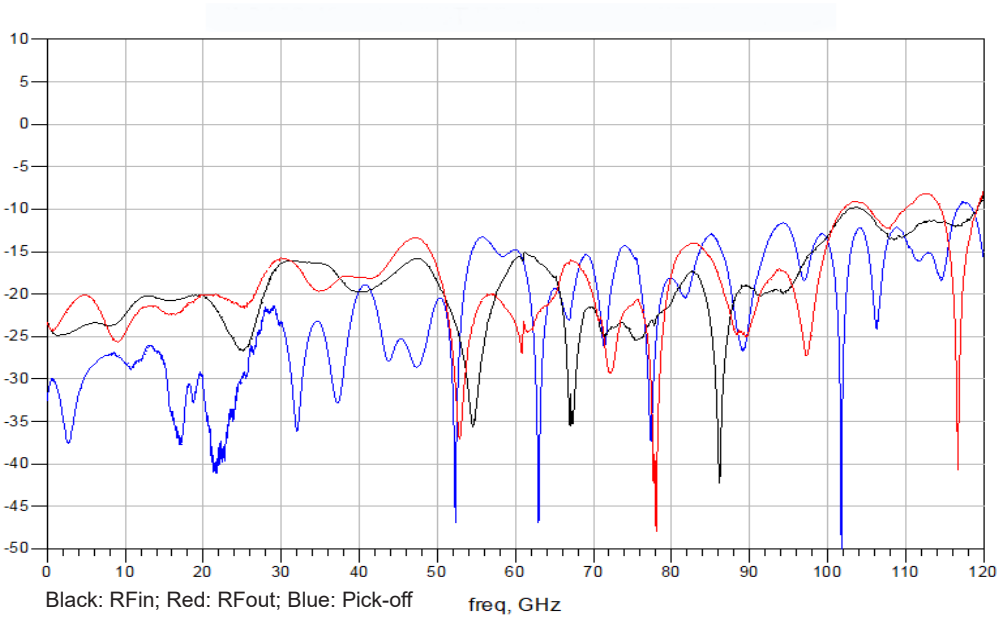


Figure 2: HL9469-PCIe8.0 Return Loss (opt. -JPJ)

HL9469-PCIe-8.0 Group Delay

Figure 3 shows typical group delay of the thru and pick-off lines of the HL9469-PCIe8.0 from DC to 110 GHz.

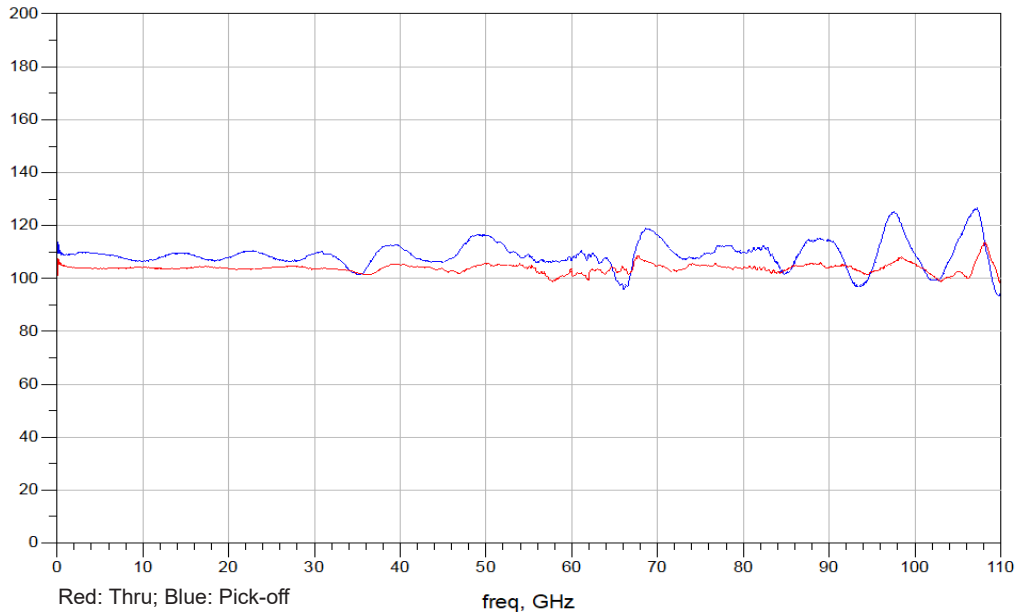


Figure 3: HL9469-PCIe8.0 Group Delay (opt. -JPJ)

HL9469-PCIe8.0 Dimensional Drawing

Figure 4 shows a mechanical drawing of an HL9469-PCIe8.0, option -JPJ. Unless otherwise noted, all units are in inches.

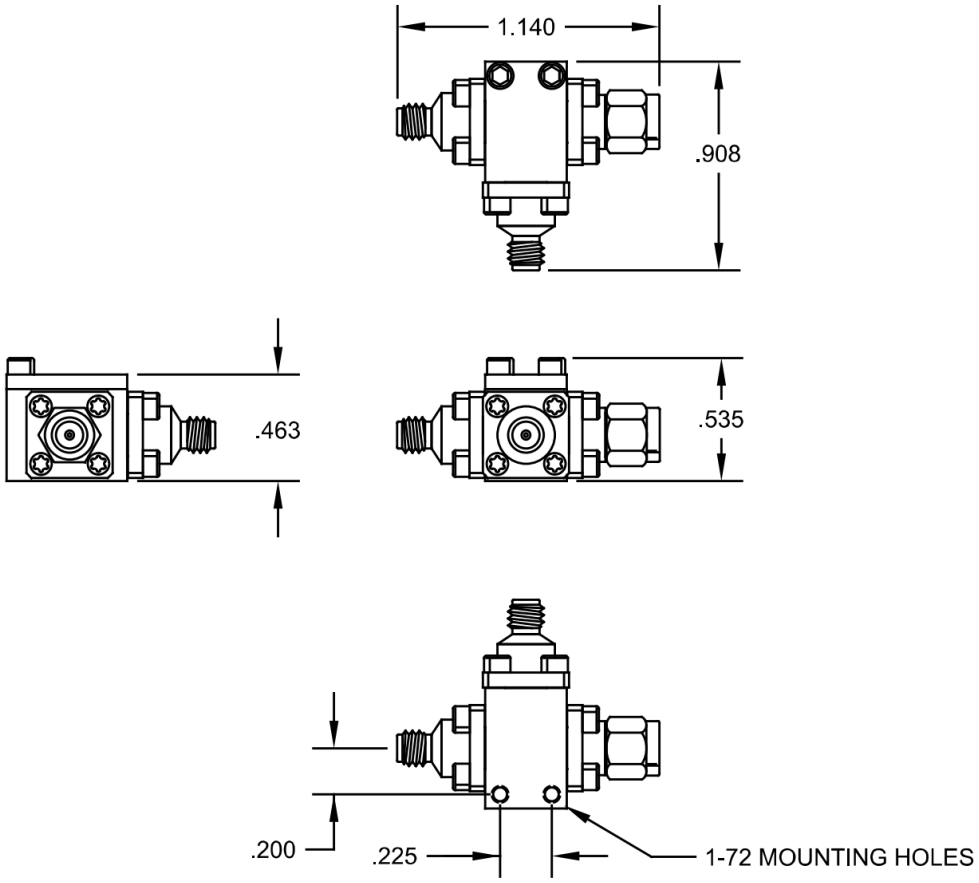


Figure 4: HL9469-PCIe8.0 mechnical drawing (opt. -JPJ)